Notice of Allowability	Application No.	Applicant(s)	
	10/617,727	YOON, JOON HO	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the request for reconsideration on 18 April 2005*.

2. ☒ The allowed claim(s) is/are *1-11*.

3. ☒ The drawings filed on *14 July 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Mary Wilczewski
Primary Examiner

DETAILED ACTION

This office action is in response to the filing of the request for reconsideration on 13 April 2005. Claims 1-11 are pending.

Response to Arguments

Applicant's arguments, see the paper filed 18 April 2005, with respect to claims 1-11 have been fully considered and are persuasive. The rejection of claims 1-11 has been withdrawn.

Allowable Subject Matter

Claims 1-11 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of manufacturing a light-emitting diode device where a lead frame including first pattern part for use in mounting a light-emitting diode chip thereon, a second pattern part electrically connected to the first pattern part to be used as an electrode, a third pattern part spaced from the first pattern part to be electrically insulated from the first pattern part and used as another electrode, and fourth pattern part and a fifth pattern part integrated with both sides of the first pattern part; plating the first, second and third pattern parts of the lead frame with a metal having high adhesion and conductivity; plating the fourth pattern part and the fifth

pattern part with another metal having high reflectivity; mounting the light-emitting diode chip on the plated first pattern part of the lead frame; wire-bonding the light-emitting diode chip mounted on the lead frame to portions of the second and third pattern parts, to form wire-bonded portions; molding the light-emitting diode chip and the wire-bonded portions so as to protect the light-emitting diode chip and the wire-bonded portions; upwardly folding the plated fourth and fifth pattern parts, neither being molded, relative to the first pattern part to allow plated surfaces of the fourth and fifth pattern parts to face each other, thus forming reflective surfaces; and forming non-molded portions of the second and third pattern parts to make leads.

For example, Usui et al. (JP 06-204569) disclose a method of manufacturing a light-emitting diode device where a lead frame is formed including a first pattern part for use in mounting a light-emitting diode (LED) chip thereon, a second pattern part electrically connected to the first pattern part to be used as an electrode, a third pattern part spaced from the first pattern part to be electrically insulated from the first pattern part and used as another electrode, and a fourth pattern part and a fifth pattern part integrated with the first pattern part; plating the fourth pattern part and the fifth pattern part with a metal having high reflectivity, to prepare plated fourth and fifth pattern parts; mounting the light-emitting diode chip on the first pattern part of the lead frame; wire-bonding the light-emitting diode chip mounted on the lead frame to portions of the second and third pattern parts, to form wire-bonded portions; molding the light-emitting diode chip and the wire-bonded portions so as to protect the light-emitting diode chip and the wire-bonded portions; upwardly folding the plated fourth and fifth pattern parts,

neither being molded, thus forming reflective surfaces; and forming non-molded portions of the second and third pattern parts to make leads. However, Usui et al. do not disclose, anticipate, teach, or suggest plating the first, second and third pattern parts of the lead frame with a metal having high adhesion and conductivity; and upwardly folding the plated fourth and fifth pattern parts, neither being molded, relative to the first pattern part to allow plated surfaces of the fourth and fifth pattern parts to face each other, thus forming reflective surfaces.

Kondo et al. (JP 2000-269556) disclose a method of manufacturing a light-emitting diode device where a lead frame is formed including a first pattern part for use in mounting a light-emitting diode (LED) chip thereon, a second pattern part electrically connected to the first pattern part to be used as an electrode, a third pattern part spaced from the first pattern part to be electrically insulated from the first pattern part and used as another electrode, and a fourth pattern part and a fifth pattern part integrated with both sides of the first pattern part; mounting the light-emitting diode chip on the first pattern part of the lead frame ; wire-bonding the light-emitting diode chip mounted on the lead frame to portions of the second and third pattern parts, to form wire-bonded portions; molding the light-emitting diode chip and the wire-bonded portions so as to protect the light-emitting diode chip and the wire-bonded portions; upwardly folding the plated fourth and fifth pattern parts; and forming non-molded portions of the second and third pattern parts to make leads. However, Kondo et al. do not disclose, anticipate, teach or suggest plating the first, second and third pattern parts of the lead frame with a metal having high adhesion and conductivity; plating the fourth pattern part and the fifth

pattern part with another metal having high reflectivity; and upwardly folding the plated fourth and fifth pattern parts, neither being molded, relative to the first pattern part to allow plated surfaces of the fourth and fifth pattern parts to face each other, thus forming reflective surfaces.

The prior art made of record in this action does not anticipate, teach, or suggest a method of manufacturing a light-emitting diode device where a lead frame including first pattern part for use in mounting a light-emitting diode chip thereon, a second pattern part electrically connected to the first pattern part to be used as an electrode, a third pattern part spaced from the first pattern part to be electrically insulated from the first pattern part and used as another electrode, and fourth pattern part and a fifth pattern part integrated with both sides of the first pattern part; plating the first, second and third pattern parts of the lead frame with a metal having high adhesion and conductivity; plating the fourth pattern part and the fifth pattern part with another metal having high reflectivity; mounting the light-emitting diode chip on the plated first pattern part of the lead frame; wire-bonding the light-emitting diode chip mounted on the lead frame to portions of the second and third pattern parts, to form wire-bonded portions; molding the light-emitting diode chip and the wire-bonded portions so as to protect the light-emitting diode chip and the wire-bonded portions; upwardly folding the plated fourth and fifth pattern parts, neither being molded, relative to the first pattern part to allow plated surfaces of the fourth and fifth pattern parts to face each other, thus forming reflective surfaces; and forming non-molded portions of the second and third pattern parts to make leads.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Mary Wilczewski
Primary Examiner